## MEGHANA BIKKI BU21EECE0100559 CADENCE REPORT

## Experiment 1: Schematic and DC Simulation of a Resistive Voltage Divider

### Introduction

This experiment involves creating a schematic of a resistive voltage divider and performing a DC simulation to analyze its behavior.

### Procedure

**Library Creation**

* Open Oracle VM VirtualBox and launch Terminal.
* Create a directory and set up the environment.
* Start Virtuoso and create a new library named mylib, attaching it to the gpdk090 technology file.

**Schematic Creation**

* Create a new cell view named voltage\_divider.
* Add resistors (R1 and R2), a voltage source (Vdc), and ground (GND) to the schematic.
* Connect the components as per the voltage divider circuit and name the wires appropriately.
* Save the schematic.

**DC Simulation Setup and Execution**

* Launch ADE L and configure DC Analysis.
* Select Vout as the output net.
* Run the simulation and view the output graphs.

### Conclusion

The schematic and DC simulation of a resistive voltage divider were successfully implemented. The simulation results were verified using the generated output graphs.

## Experiment 2: Schematic and Transient Analysis of a First Order RC Circuit

### Introduction

This experiment involves creating a schematic of a first-order RC circuit and performing a transient analysis to observe its behavior over time.

### Procedure

**Library Creation**

* Open Oracle VM VirtualBox and launch Terminal.
* Create a directory and set up the environment.
* Start Virtuoso and create a new library named mylib, attaching it to the gpdk090 technology file.

**Schematic Creation**

* Create a new cell view named rc\_circuit.
* Add a resistor (R), a capacitor (C), a pulse voltage source (Vpulse), and ground (GND) to the schematic.
* Connect the components as per the RC circuit and name the wires appropriately.
* Save the schematic.

**Transient Analysis Setup and Execution**

* Launch ADE L and configure Transient Analysis with a stop time of 2ms.
* Select Vout as the output net.
* Run the simulation and view the output graphs.

### Conclusion

The schematic and transient analysis of a first-order RC circuit were successfully implemented. The simulation results were verified using the generated output graphs.

## Experiment 3: Study and Simulation of Operating Regions of a MOSFET

### Introduction

This experiment involves studying and simulating the operating regions of a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor).

### Procedure

**Library Creation**

* Open Oracle VM VirtualBox and launch Terminal.
* Create a directory and set up the environment.
* Start Virtuoso and create a new library named mylib, attaching it to the gpdk090 technology file.

**Schematic Creation**

* Create a new cell view named mosfet\_study.
* Add an NMOS transistor, a DC voltage source (Vdc), and ground (GND) to the schematic.
* Connect the components as per the MOSFET test circuit and name the wires appropriately.
* Save the schematic.

**DC Simulation Setup and Execution**

* Launch ADE L and configure DC Analysis.
* Select Ids as the output net.
* Run the simulation and view the output graphs.

### Conclusion

The study and simulation of the operating regions of a MOSFET were successfully implemented. The simulation results were verified using the generated output graphs.

## Experiment 4: Schematic, Symbol, and Simulation of a CMOS Inverter

### Introduction

This experiment involves creating a schematic, symbol, and simulation of a CMOS inverter.

### Procedure

**Library Creation**

* Open Oracle VM VirtualBox and launch Terminal.
* Create a directory and set up the environment.
* Start Virtuoso and create a new library named mylib, attaching it to the gpdk090 technology file.

**Schematic Creation**

* Create a new cell view named cmos\_inverter.
* Add an NMOS transistor, a PMOS transistor, a DC voltage source (Vdc), and ground (GND) to the schematic.
* Connect the components as per the CMOS inverter circuit and name the wires appropriately.
* Save the schematic.

**Symbol Creation**

* Create a symbol for the CMOS inverter from the schematic view.

**Transient Simulation Setup and Execution**

* Launch ADE L and configure Transient Analysis with a stop time of 100ns.
* Select Vout as the output net.
* Run the simulation and view the output graphs.

### Conclusion

The schematic, symbol, and simulation of a CMOS inverter were successfully implemented. The simulation results were verified using the generated output graphs.

## Experiment 5: Layout, DRC, LVS of a CMOS Inverter

### Introduction

This experiment involves creating the layout, performing Design Rule Check (DRC), and Layout Versus Schematic (LVS) check of a CMOS inverter.

### Procedure

**Library Creation**

* Open Oracle VM VirtualBox and launch Terminal.
* Create a directory and set up the environment.
* Start Virtuoso and create a new library named mylib, attaching it to the gpdk090 technology file.

**Layout Creation**

* Create a new cell view named cmos\_inverter\_layout with a layout view.
* Add NMOS and PMOS transistors and create the layout for the CMOS inverter using appropriate layers and connections.

**Design Rule Check (DRC)**

* Verify the layout against design rules and fix any errors found.

**Layout Versus Schematic (LVS)**

* Compare the layout with the schematic and fix any discrepancies found.

### Conclusion

The layout, DRC, and LVS of a CMOS inverter were successfully implemented. The design passed the DRC and LVS checks, ensuring that the layout matches the schematic.

## Experiment 6: Hierarchical Schematic and Simulation of a NAND, XOR, and 1-bit Full Adder

### Introduction

This experiment involves creating hierarchical schematics and simulations for a NAND gate, XOR gate, and a 1-bit full adder.

### Procedure

**Library Creation**

* Open Oracle VM VirtualBox and launch Terminal.
* Create a directory and set up the environment.
* Start Virtuoso and create a new library named mylib, attaching it to the gpdk090 technology file.

**Schematic Creation**

* Create cell views for nand\_gate, xor\_gate, and full\_adder.
* Add the necessary components (NMOS and PMOS transistors) and connect them as per the logic circuits for NAND, XOR, and full adder.
* Name the wires appropriately and save the schematics.

**Symbol Creation**

* Create symbols for each logic gate from the schematic views.

**Hierarchical Schematic for Full Adder**

* Create a new cell view for the hierarchical full adder.
* Instantiate the NAND and XOR gate symbols and connect them to form a 1-bit full adder.

**Simulation Setup and Execution**

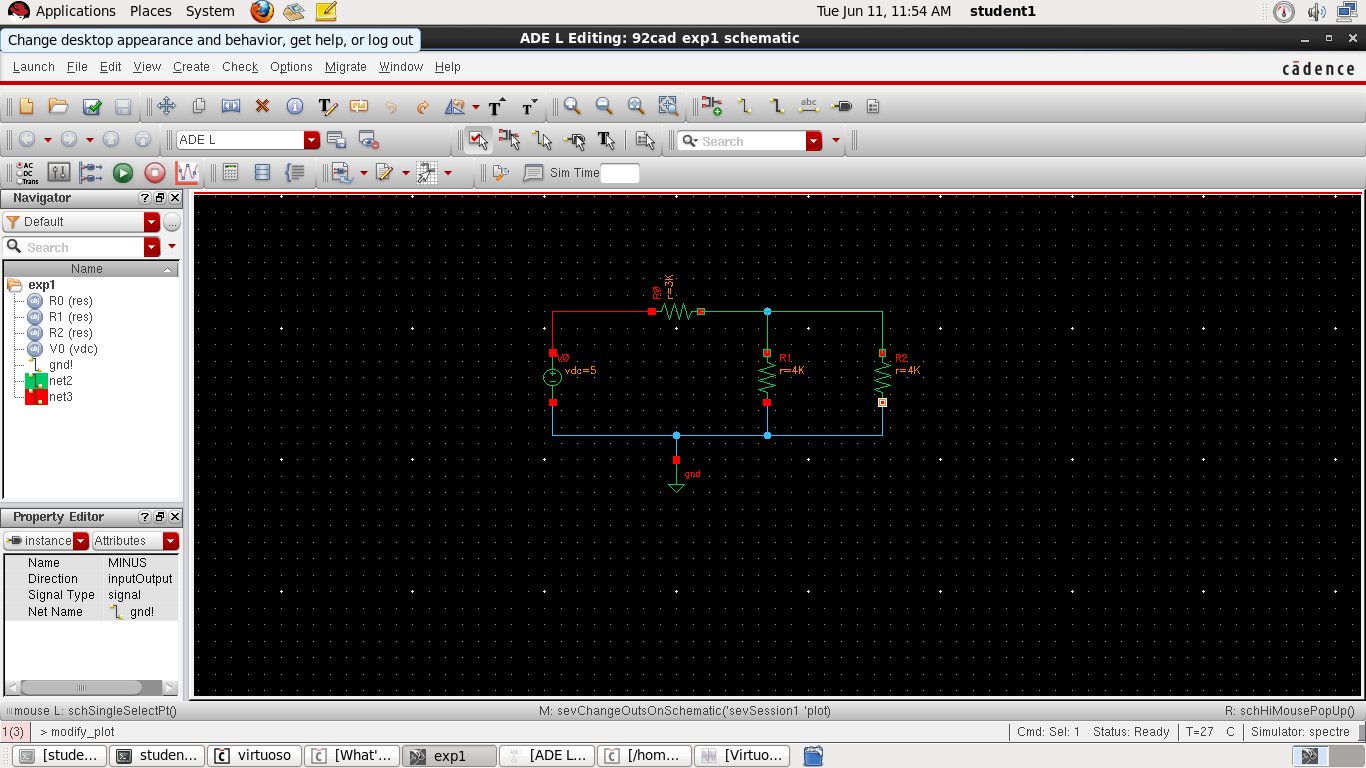
* Launch ADE L and configure the appropriate analysis (transient or DC).
* Select the output nets and run the simulations.
* View the output graphs to verify the functionality.

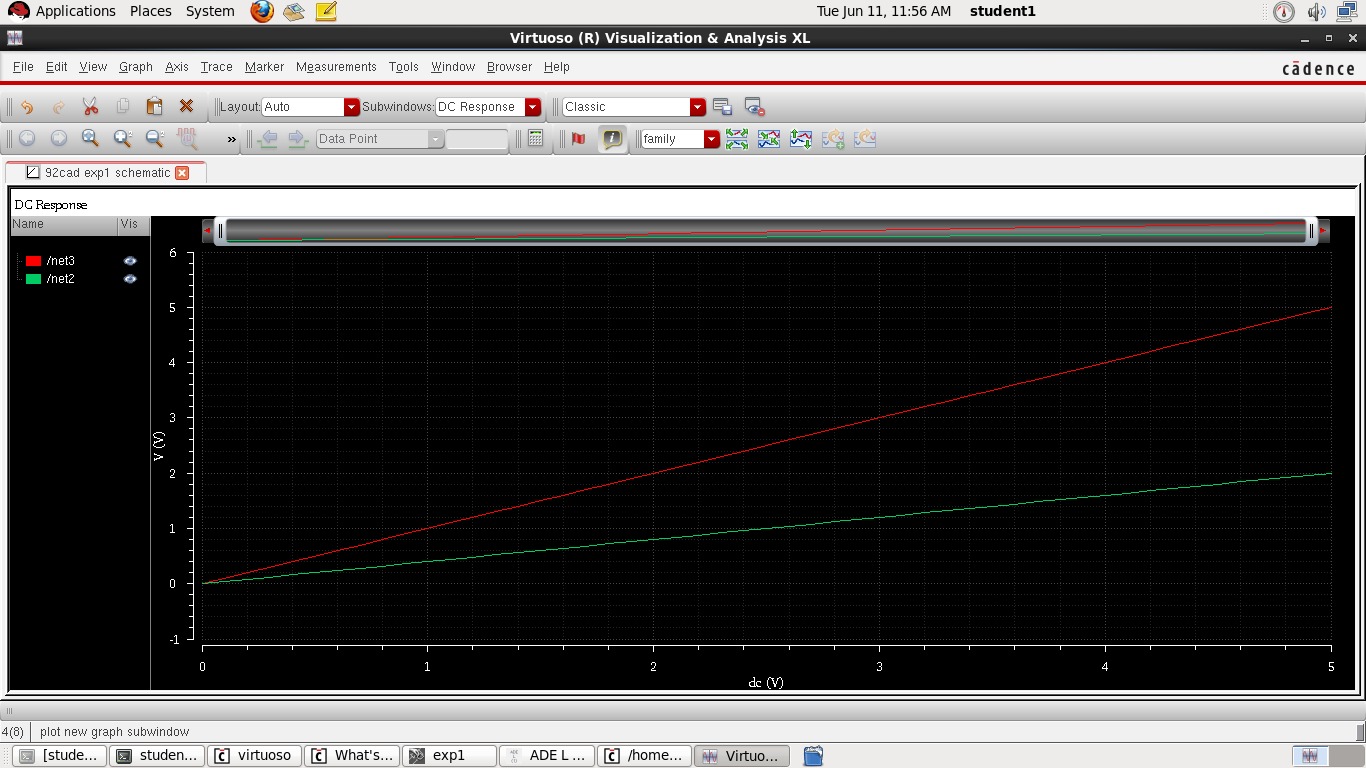
### Conclusion

The hierarchical schematics and simulations for the NAND gate, XOR gate, and 1-bit full adder were successfully implemented. The simulation results were verified using the generated output graphs.

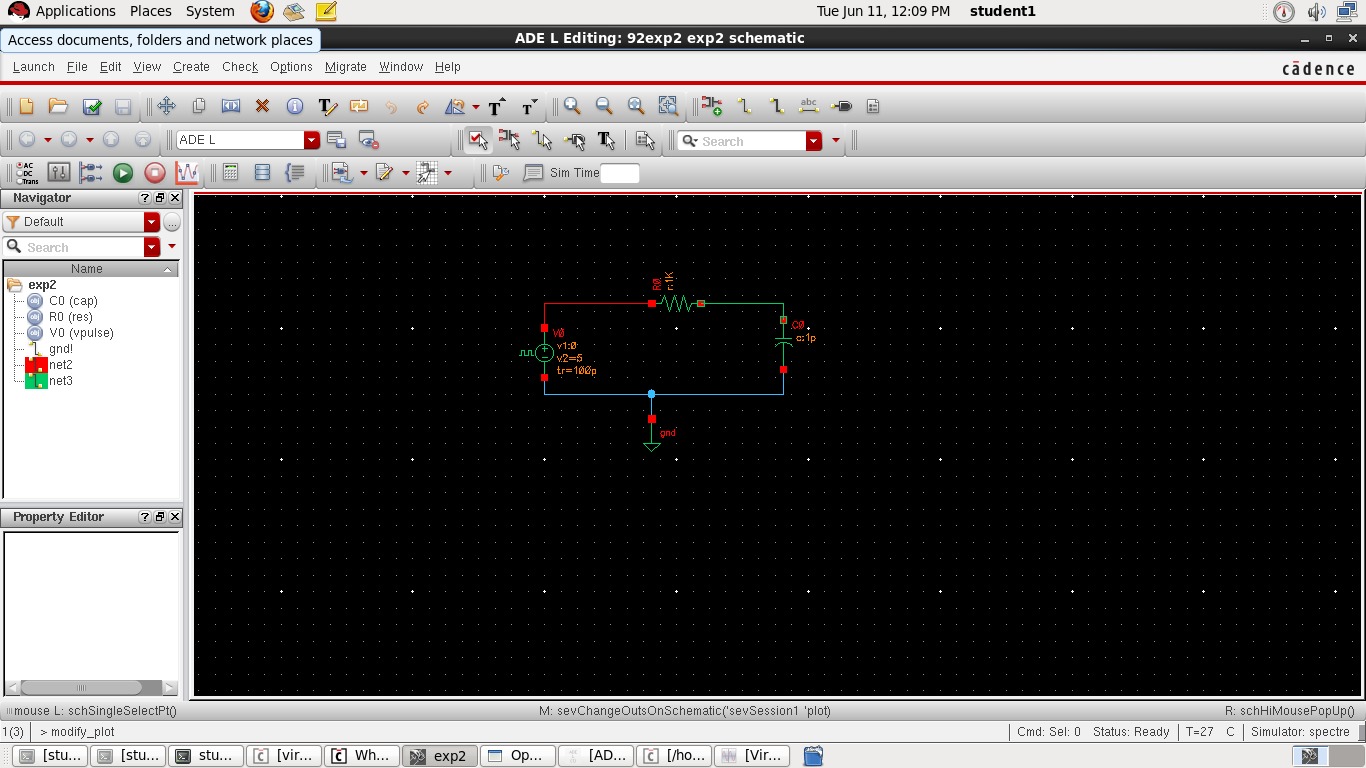
**EXPERIMENT SCREENSHOTS:**

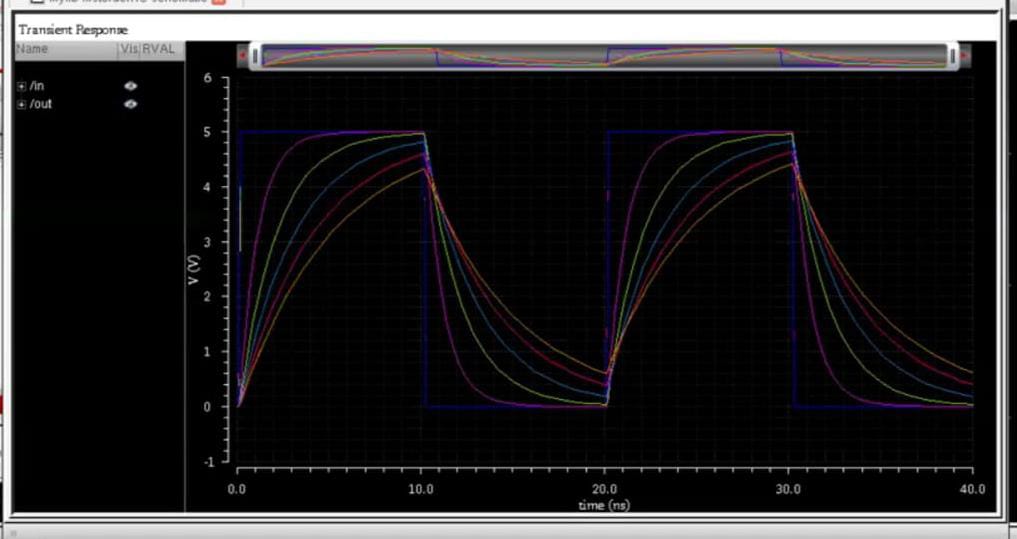
**Experiment one circuit and outputs:**

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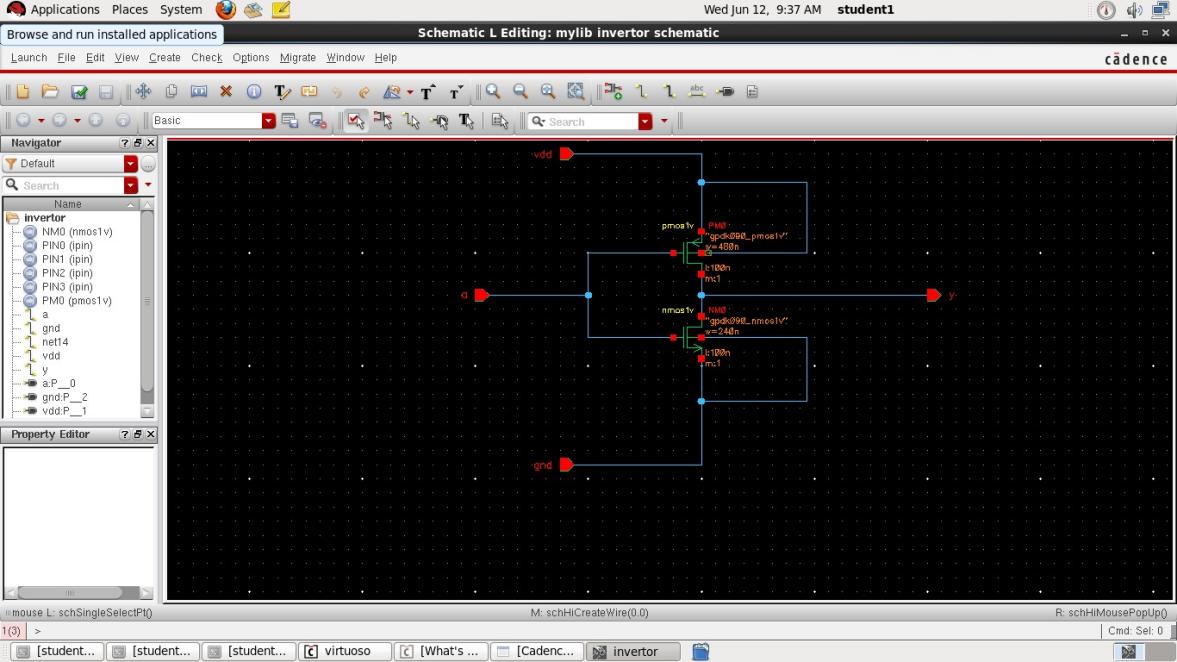


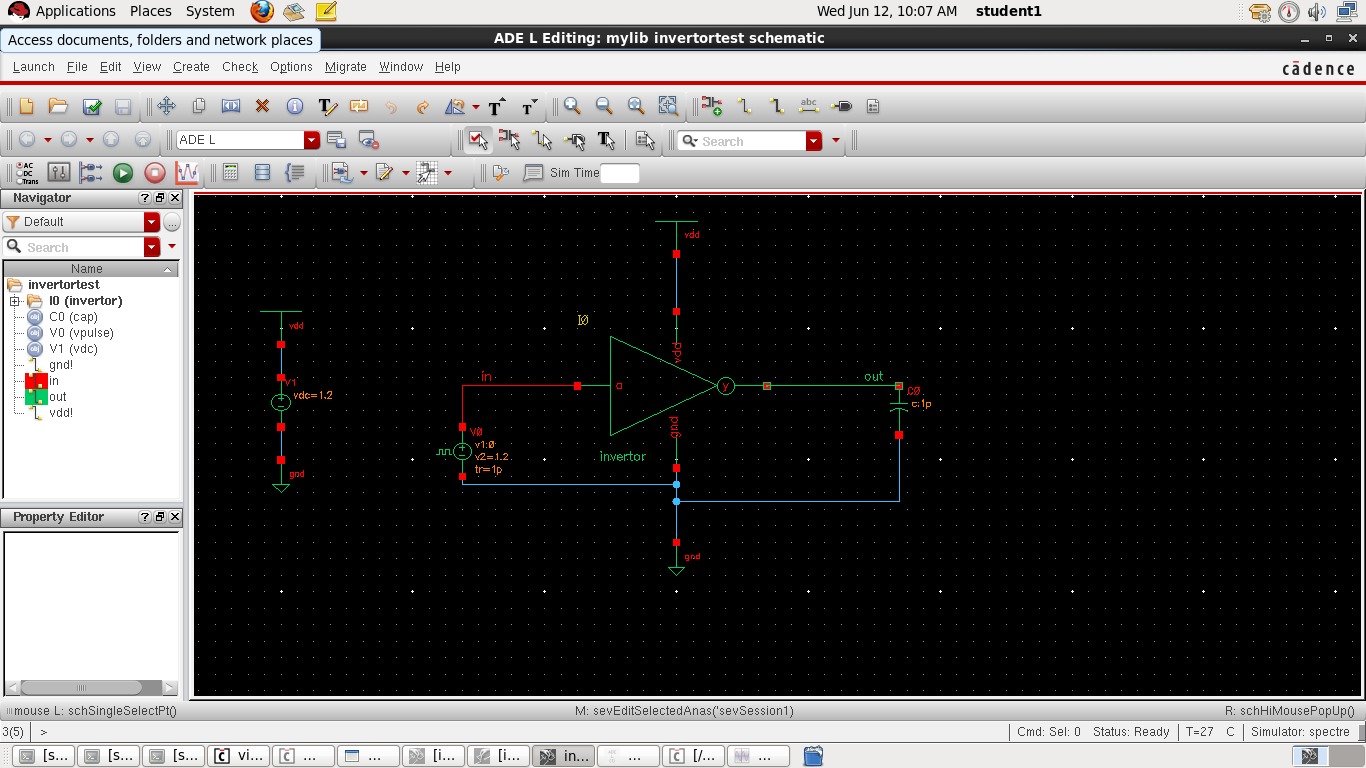
**Experiment two circuit and outputs:**

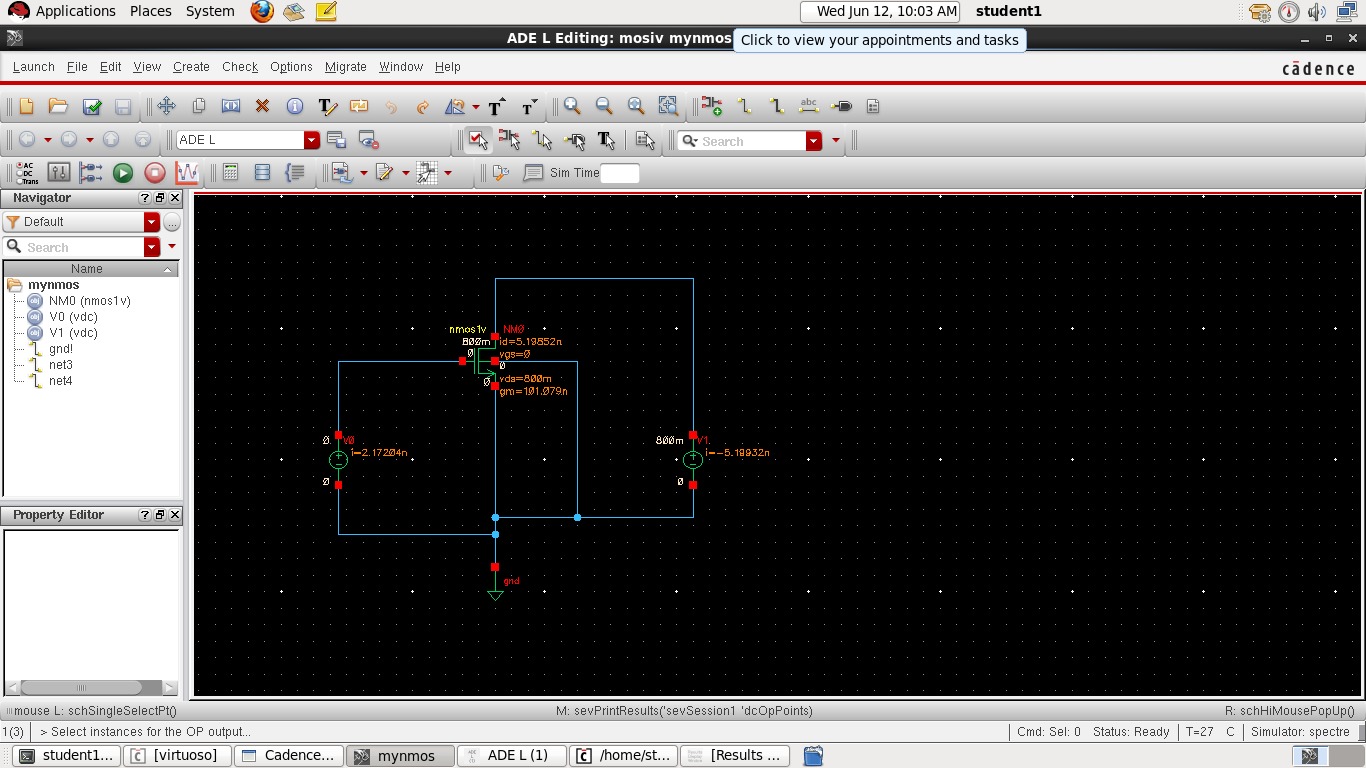
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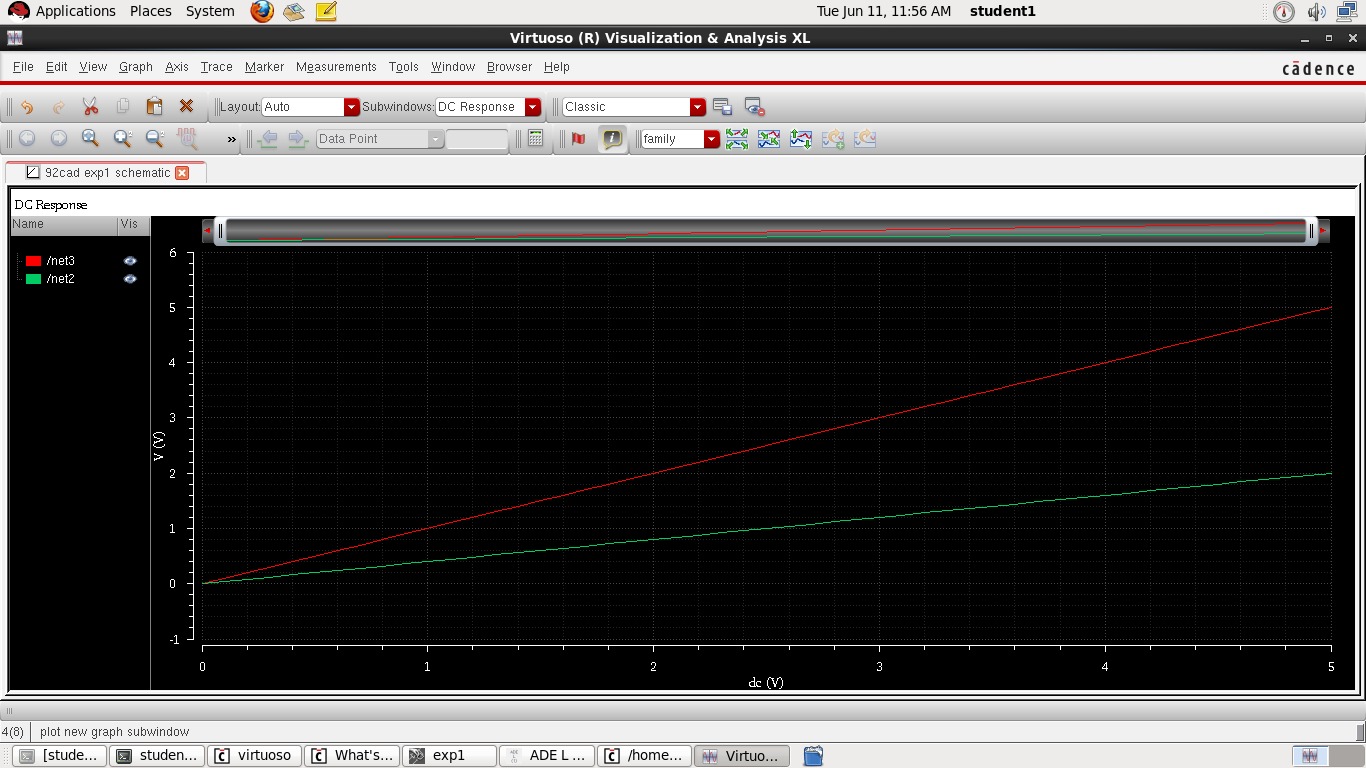
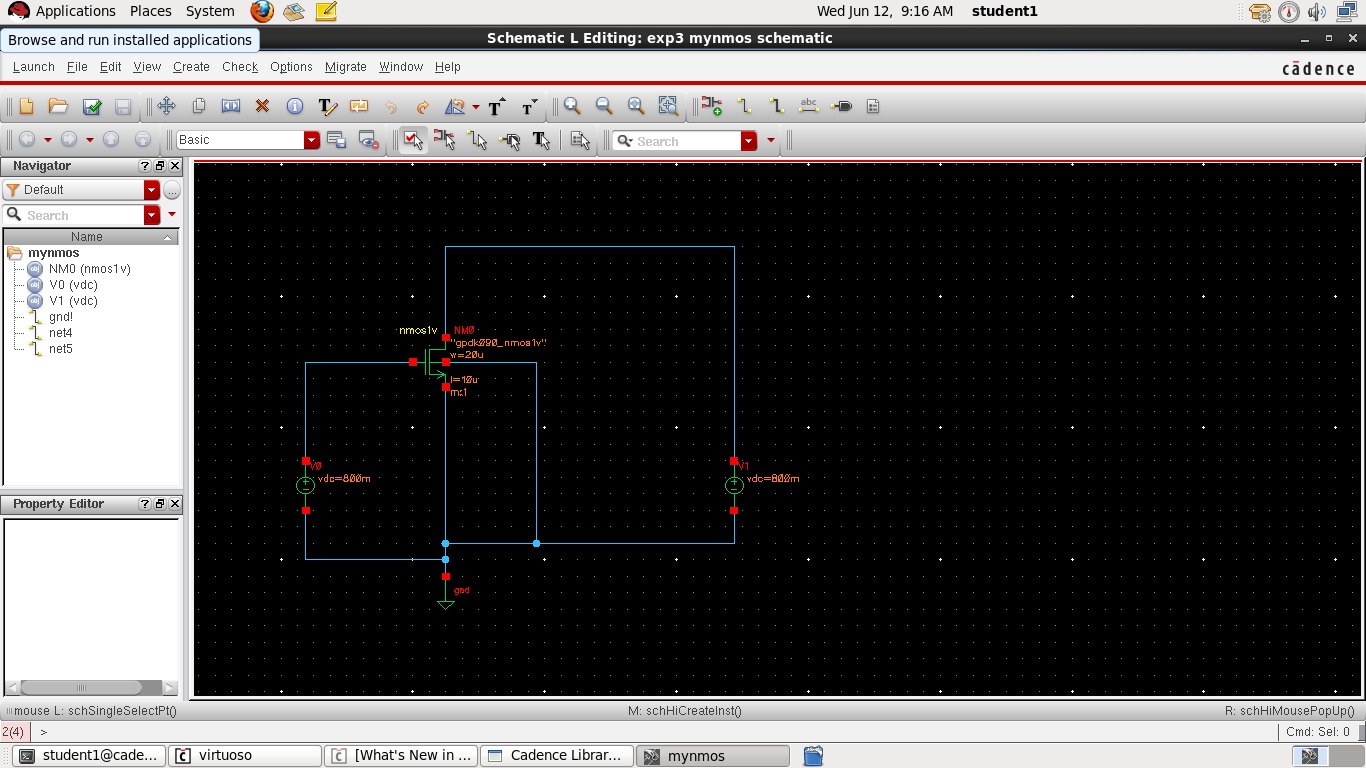
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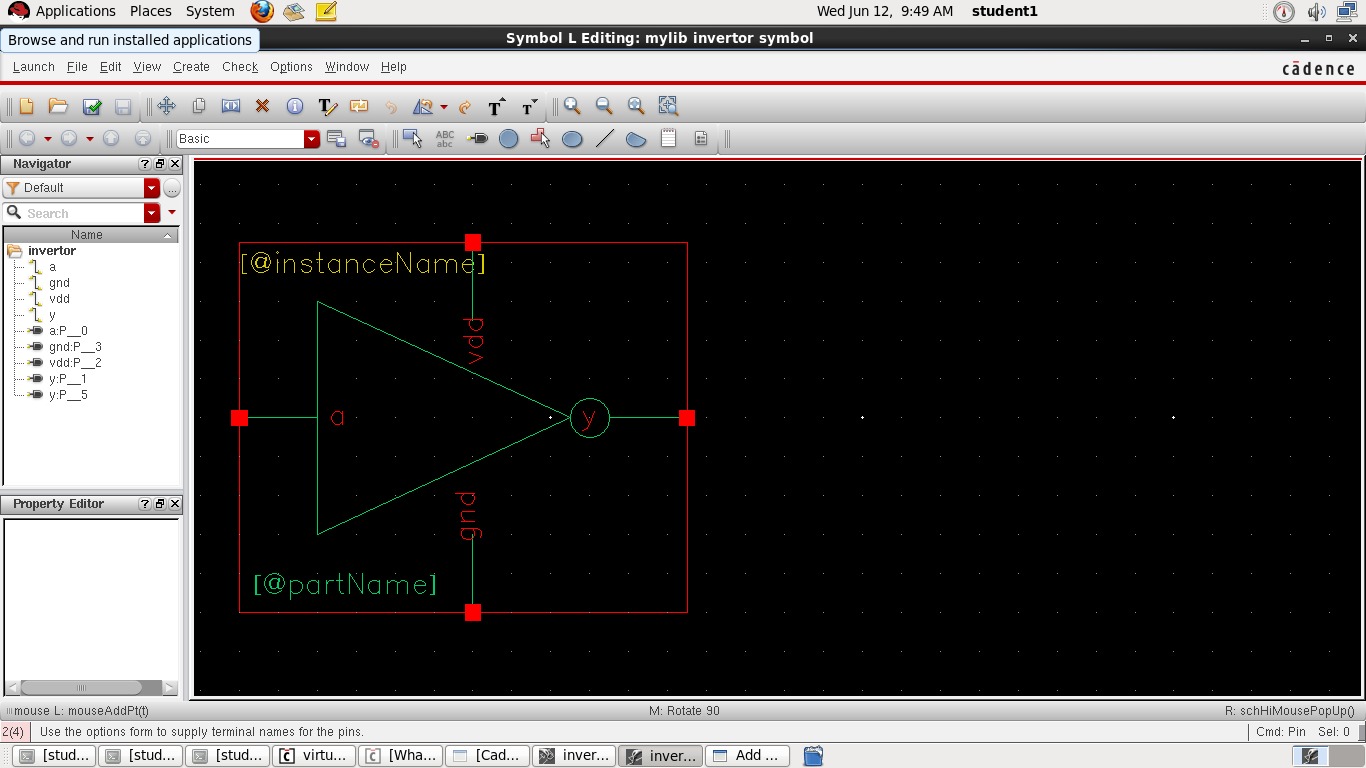
**Experiment three & four circuit--outputs:**

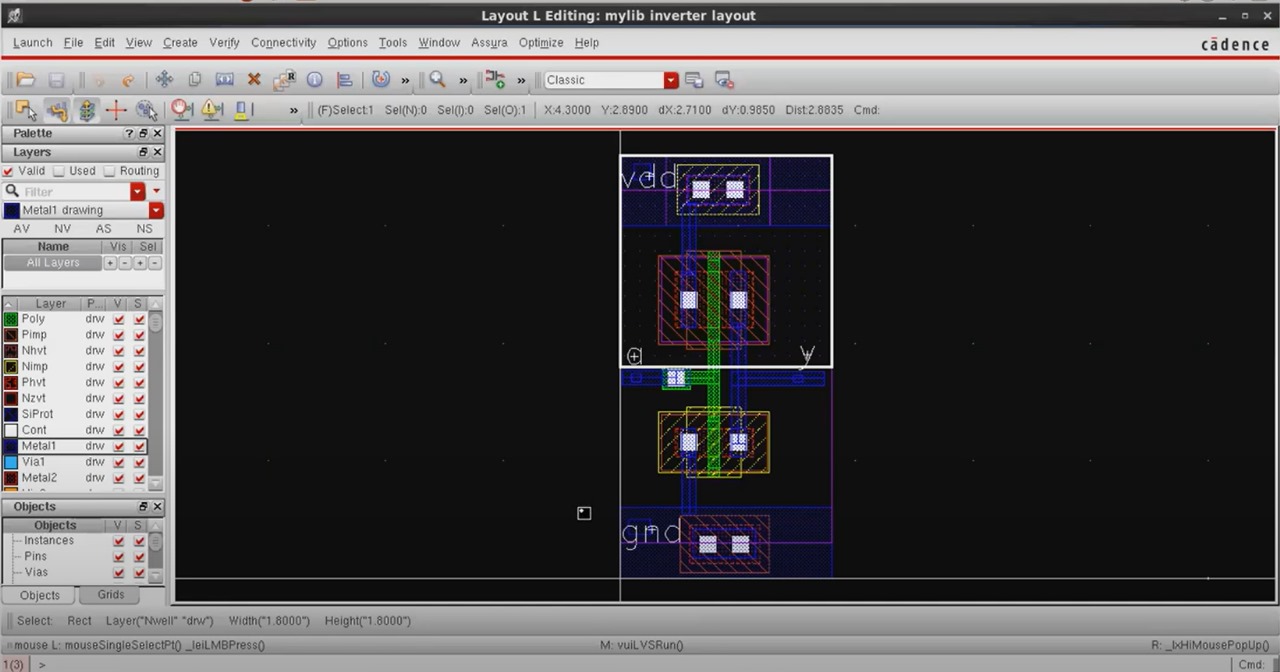
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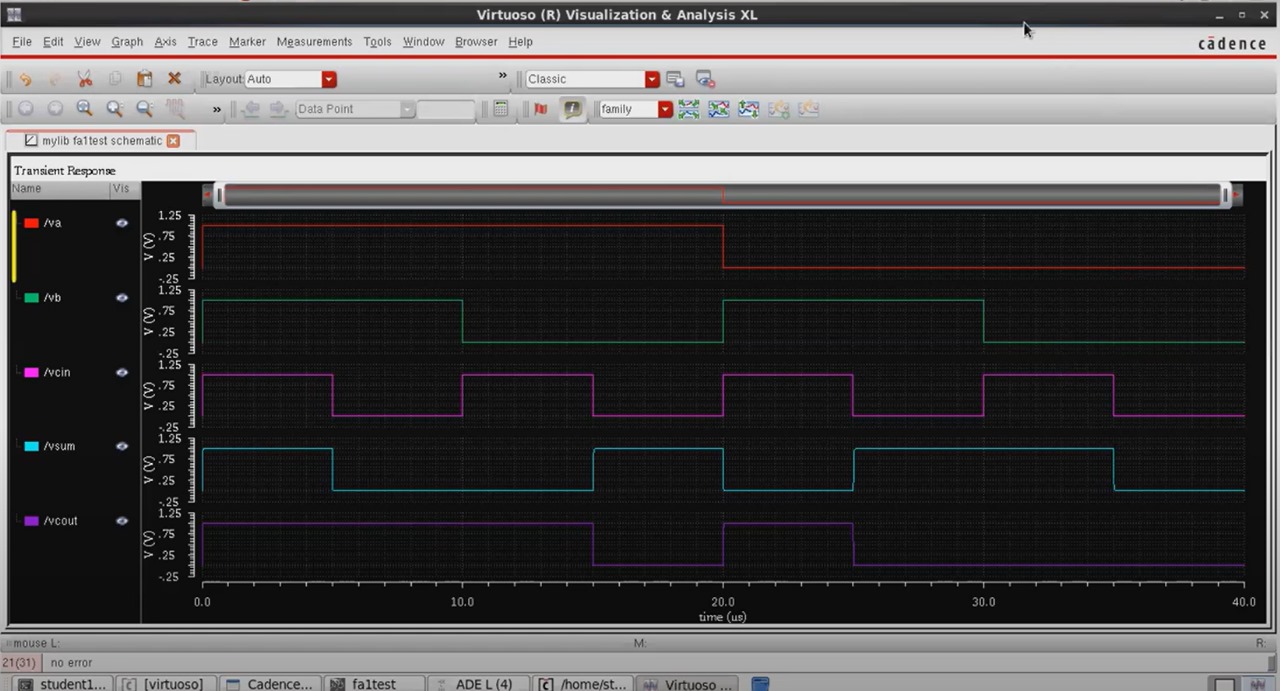




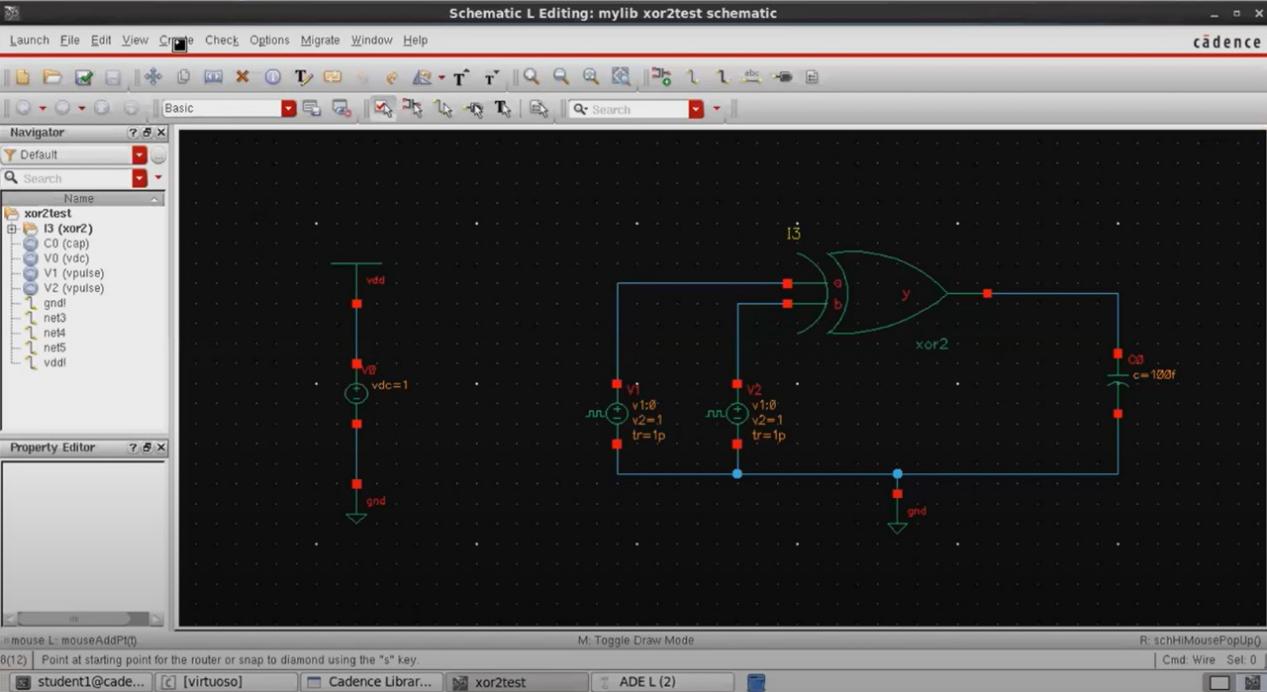


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**Experiment five circuit--outputs:**



**Experiment six circuit--outputs:**

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